# Ge-On-Insulator substrates obtained by Ge condensation technique: Fabrication, modelisation and electrical characterization

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## 1. Introduction

Silicon Germanium On Insulator (SGOI) is a straightforward material for ultimate device scaling. This substrate combines two advantages: high carrier velocity of the $Si_{1-x}Ge_x$ alloy and low parasitic capacitance due to the presence of a buried oxide. Several fabrication techniques for SGOI substrates, as SIMOX, SMART-CUT™ or Liquid Phase Epitaxy [1] have been proposed. Tezuka *et al.* [2] have presented a new approach involving an epitaxial growth of low Ge contents SiGe alloys on a SOI substrate followed by a high temperature oxidation. By selective oxidation of Silicon and diffusion of Germanium within the remaining SGOI layer, Ge content increases. A high Ge concentration SGOI layer is then obtained.

Ge condensation technique is based on two competitive mechanisms: Si selective oxidation involving a Ge pill-up at the oxide interface and Ge diffusion within the SiGe layer. Both take place during the high temperature oxidation.

In this paper, we present the fabrication procedure we have developed to obtain high quality GeOI substrates. Then

## 2. Fabrication Procedure :

A pseudomorphic $Si_{0.9}Ge_{0.1}$ layer, 75nm thick, is grown by Reduced Pressure Chemical Vapor Deposition (RPCVD) on commercial SOI wafers. A 2nm cap Si layer is added to prevent any Ge consumption during the first oxidation stages. Wafers are then thermally oxidized under a dry $O_2$ atmosphere. First oxidations done at $T_1$=1050°C are limited to a final Ge content of 65% corresponding to the SiGe melting point [3]. A second oxidation step ($T_2$=900°C) is then added to reach higher Ge contents. Figure 1 shows the experimental Ge enrichment kinetic during the whole oxidation (black dots).

Our improvements performed on the process permit to enhance Ge diffusion within the remaining SGOI layer and then homogenize the Ge content through the layer depth. SIMS measurements (not shown here) have confirmed the uniformity of the layers obtained by the improved condensation technique. 10nm homogeneous SGOI layers with Ge contents between 98 and 100% have then been obtained by this way. Ge conservation during the whole oxidation treatment has also been demonstrated.

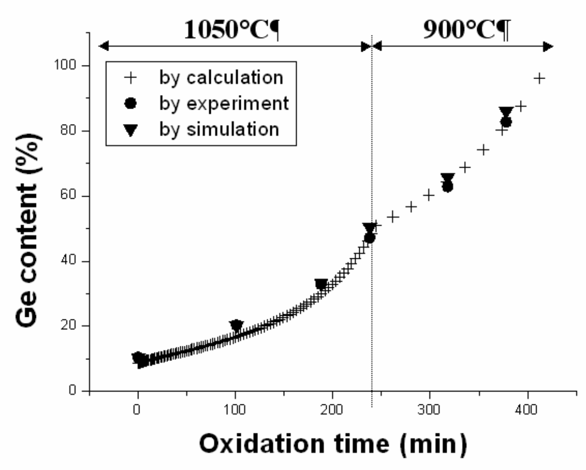

*Fig 1: Final Ge content of the SGOI layer obtained by condensation as a function of the oxidation time. Two oxidation temperatures are used to reach high Ge content.*

## 3. Ge enrichment predictions:

Numerical simulations using the Athena software [4] (fig 1-black triangles) and analytical models (fig1–black crosses) have been studied to predict Ge enrichments kinetics starting from the experimental initial parameters, i.e. top SOI thickness, SiGe grown layer thickness and compositions. Oxidation kinetics rules have firstly been identified by extraction of Deal&Grove coefficients adapted to SiGe oxidation. Then the Ge enrichments have been deduced from the oxidation kinetics by SiGe thickness predictions and Ge conservation. Zangenberg's coefficients [5] have been used to simulate the Ge diffusion through the SGOI layer. Simulation kinetics results, either by the numerical or the analytical model, are in good agreement with experimental ones.

## 4. Epitaxial regrowth on GeOI wafers

Today, ultra thin GeOI are not adapted for MOSFET fabrication due to a Ge consumption which may occur during wet processes. Therefore, the capability to regrow Ge layer on SGOI and GeOI substrates is an important issue and motivates our work. Figure 2 shows the evolution of the RMS roughness extracted from 5x5 µm² AFM pictures as a function of the bake temperature. Due to the 2D-3D morphology shift, the local roughness obviously increases with the bake temperature. Focusing on the low bake temperature area (figure inset) the RMS roughness reaches a minimum value for a bake temperature of 600°C. The same behavior is observed on global roughness measurements performed with the SP2 tool (not presented here). The optimum temperature is then determined by using this criterion.

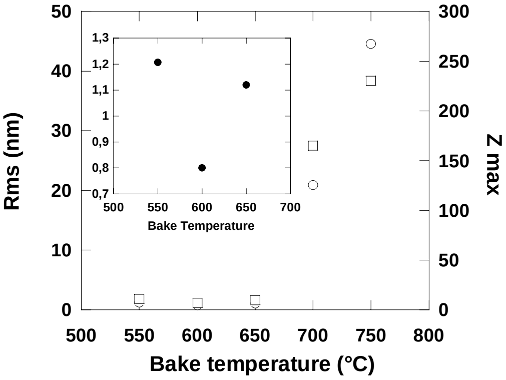

*Fig 2. Rms Roughness (circles) and Zmax in nm (squares) extracted from AFM pictures of the GeOI layers as a function of the bake temperature*

### 5- Electrical results:

Two sets of GeOI wafers with different Ge layer thicknesses, 10 nm and 100 nm, have been analyzed. The thick Ge films (100nm) were prepared by thickening the GeOI layers using Ge epitaxial regrowth after condensation. Square-shape islands (8x8 mm$^2$) were etched on the conductive film down to the buried oxide. Electrical characterization was carried out by Pseudo-MOSFET (ψ-MOS), which is a very simple and efficient method to characterize the Ge-buried oxide interface [6]. This method uses the natural upside-down MOS configuration of the structure. The GeOI film serves as the transistor body and buried oxide (BOX) acts as gate oxide. The substrate bias $V_G$ induces a conducting channel (inversion or accumulation) at the film-BOX interface. Two pressure-adjustable probes form the source and drain. The low-field mobility $\mu_0$ is extracted by drawing $I_D/g_m^{0.5}$ as a function of $V_G$ . These GeOI wafers were compared to unstrained and strained SOI materials.

Typical Ψ-MOS current is shown in figure 3. They are well behaved, with low leakage current, enabling an accurate extraction of the carrier mobility. Our 100-nm thick GeOI wafers feature an exceptional high hole mobility, beyond 400 *cm$^2$/V.s*, which exceeds recently reported values [7]. The mobility enhancement over unstrained and strained SOI is 350% and 175%, respectively.

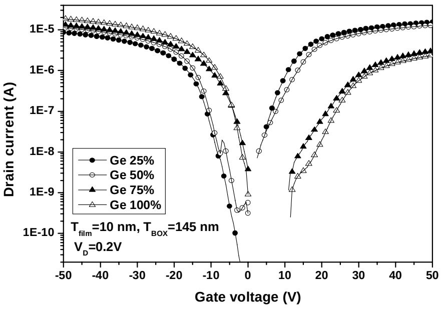

*Fig. 3. Drain current versus gate voltage in 10-nm SGOI films with different Ge percentage. Note the opposite variations in drain current for electrons and holes as the Ge content increases*

### 4. Conclusions

Uniforms SGOI substrates have been obtained with different Ge contents by improved Ge condensation technique. Experimental results are in accordance with simulations predictions. Understanding of each parameter importance and control of SiGe relaxation are under investigation. Devices fabrication on SGOI substrates with different Ge contents carried out by Ge condensation has recently been done. Electrical characterization of these samples show an exceptional high hole mobility.

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